

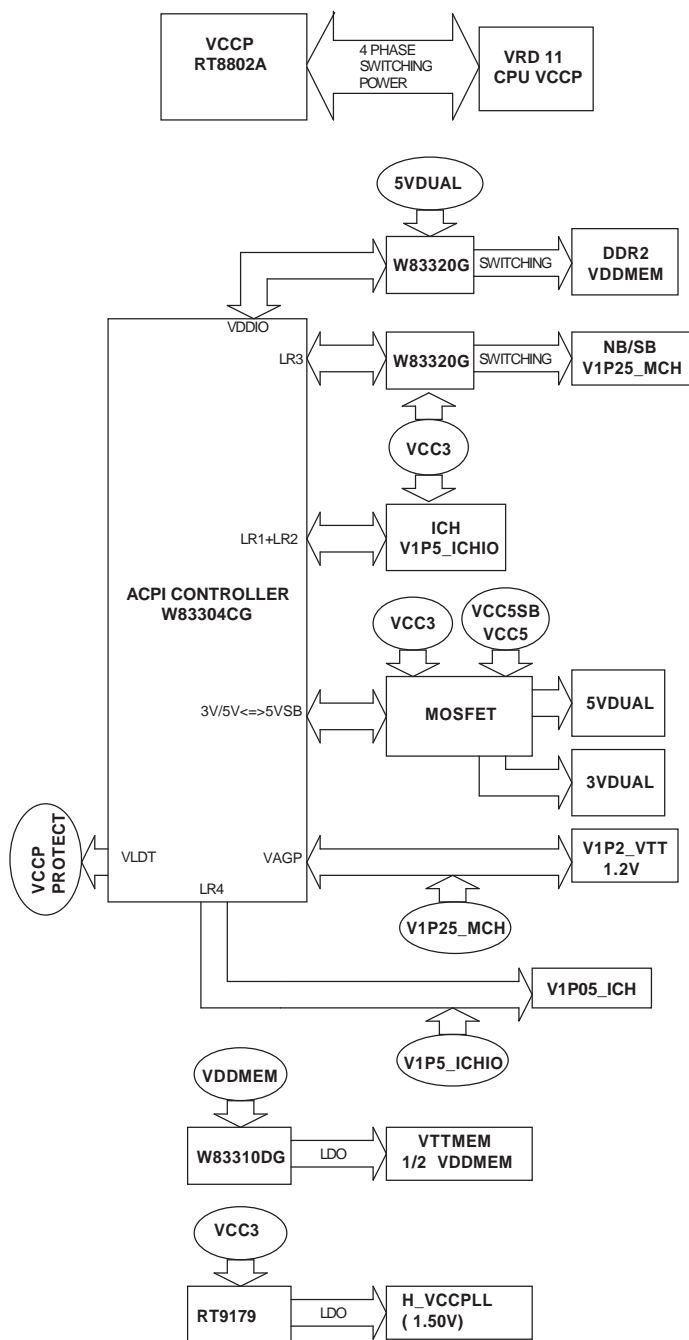
ABIT - M630 SCHEMATICS

Version: 0.22

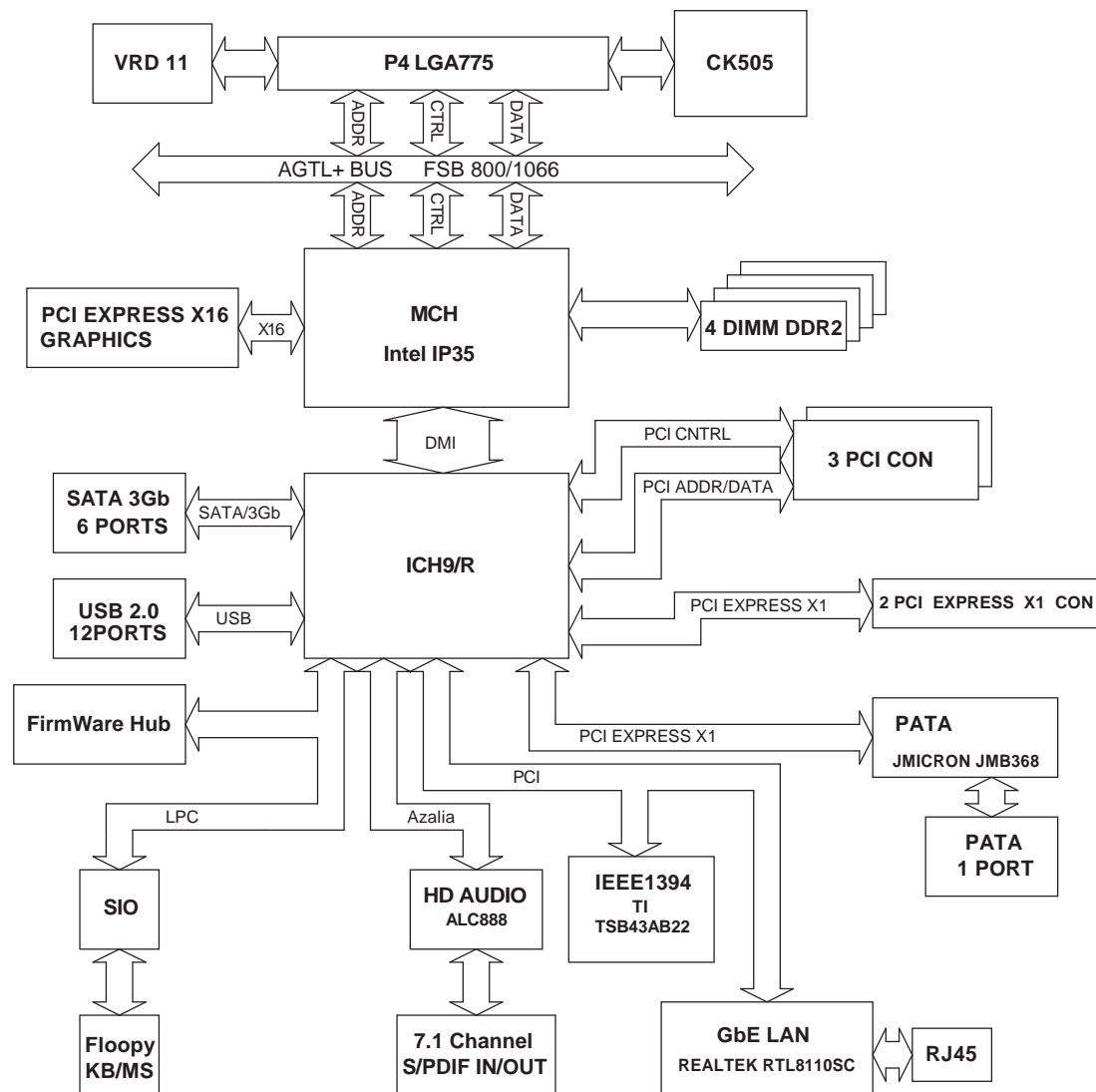
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Model	Features
IP35/IP35-E	Silent OTES 2, Dual DDR2 800 PATA, GbE, (IEEE-1394 IP35 only) 7.1-Channel HD Audio

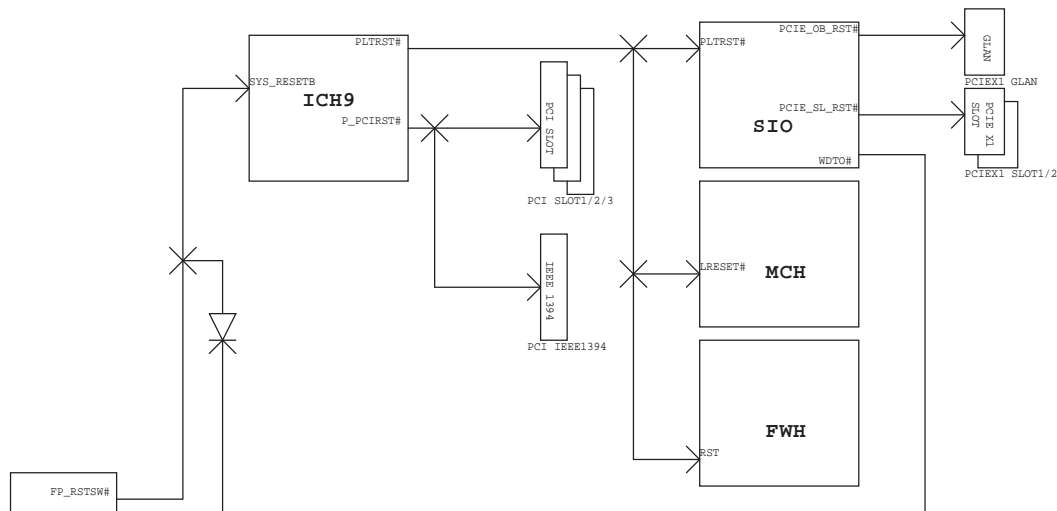
POWER DESIGN DIAGRAM



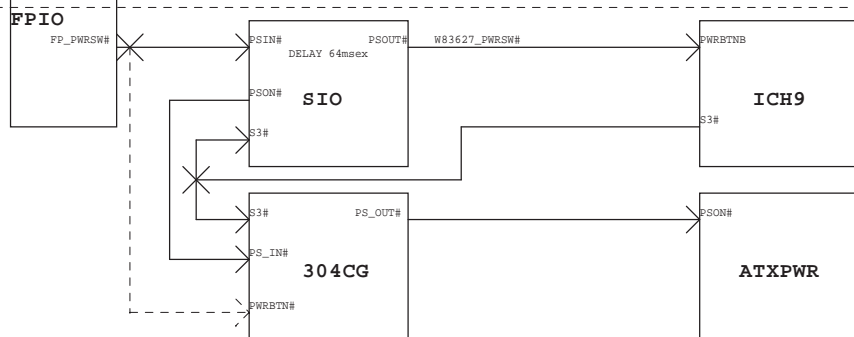
BLOCK DIAGRAM



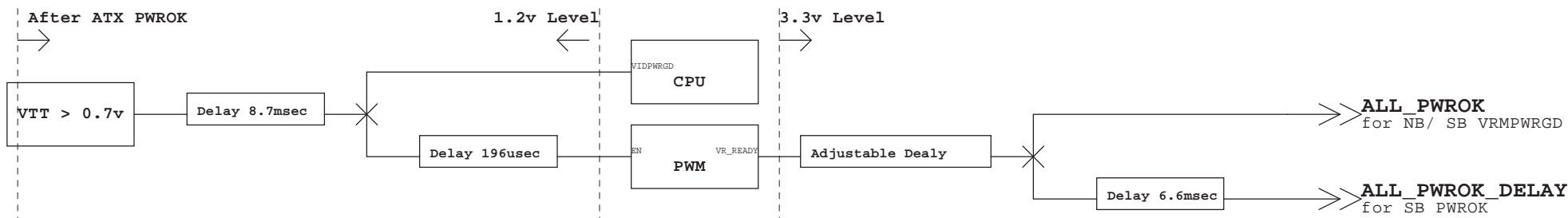
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RESET MAP



PWRON MAP



Chipset PWROK SEQ

PCI BUS ROUTE	1394	PCI1	PCI2	PCI3
IDSEL	18	19	20	21
REQ/GNT	0	1	2	3
INTA	PIRQ#E	PIRQ#F	PIRQ#G	PIRQ#H
INTB	X	PIRQ#G	PIRQ#H	PIRQ#F
INTC	X	PIRQ#H	PIRQ#F	PIRQ#G
INTD	X	PIRQ#E	PIRQ#E	PIRQ#E

PCIE BUS ROUTE	G-LAN	JMB363	PCIE1	PCIE2	PCIE X16
SOURCE	SB	SB	SB	SB	NB
BUS #	3	2	1	4	0~15

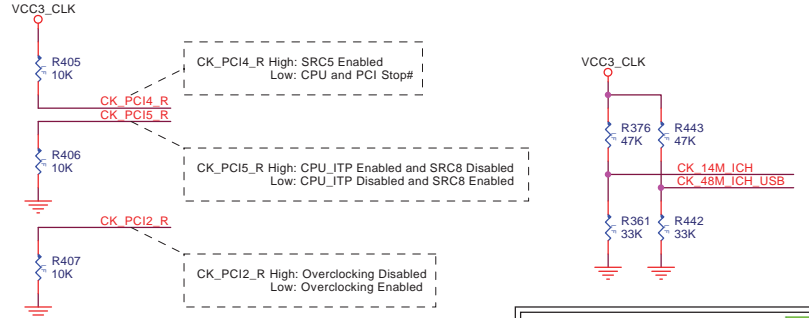
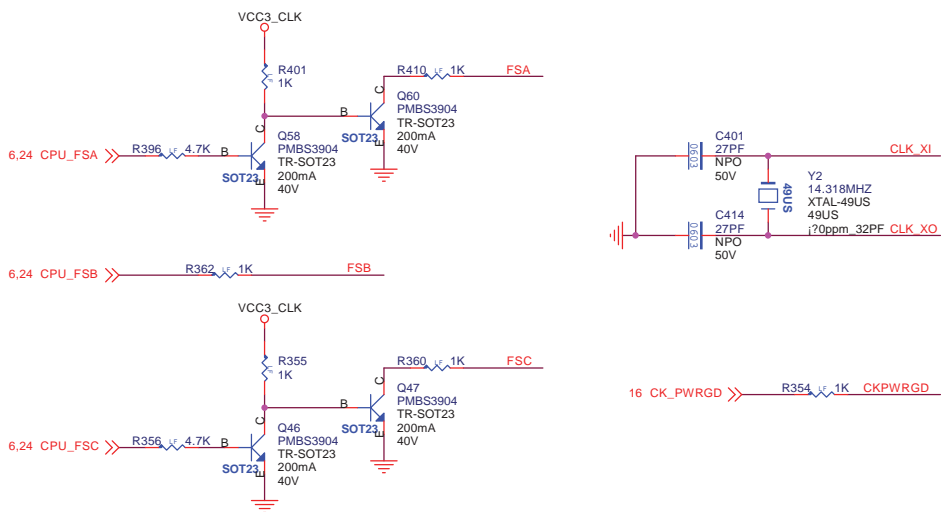
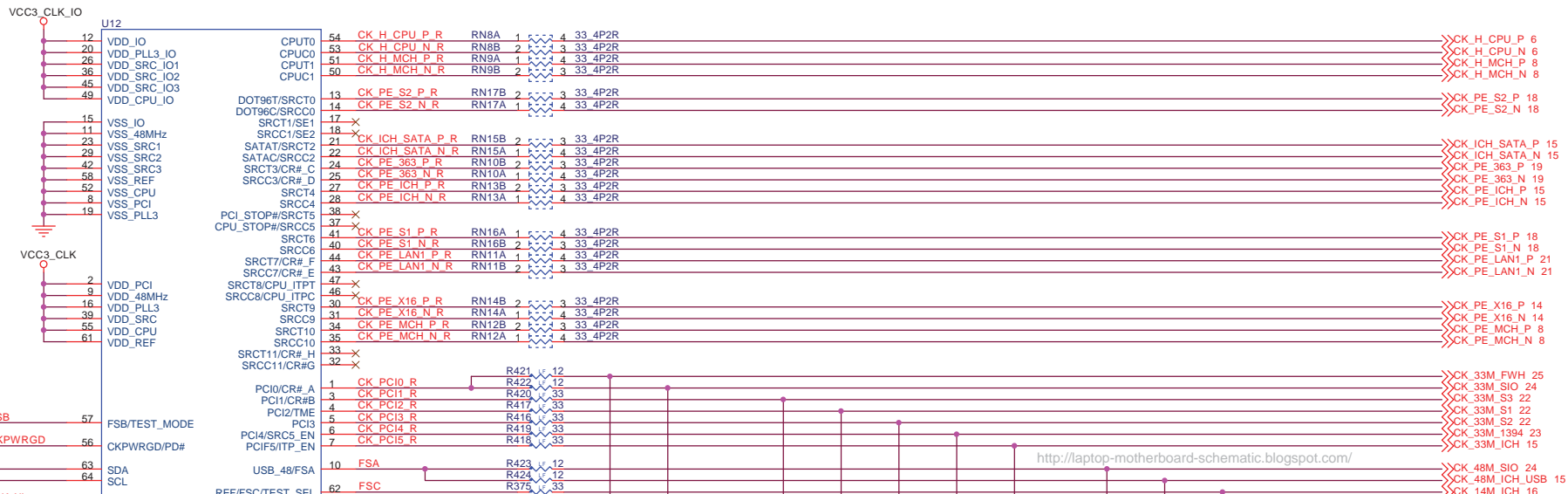
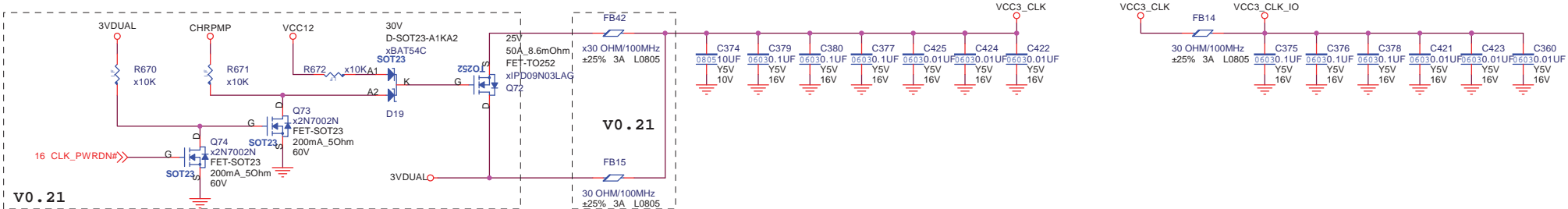
CLK GROUP1 ROUTE

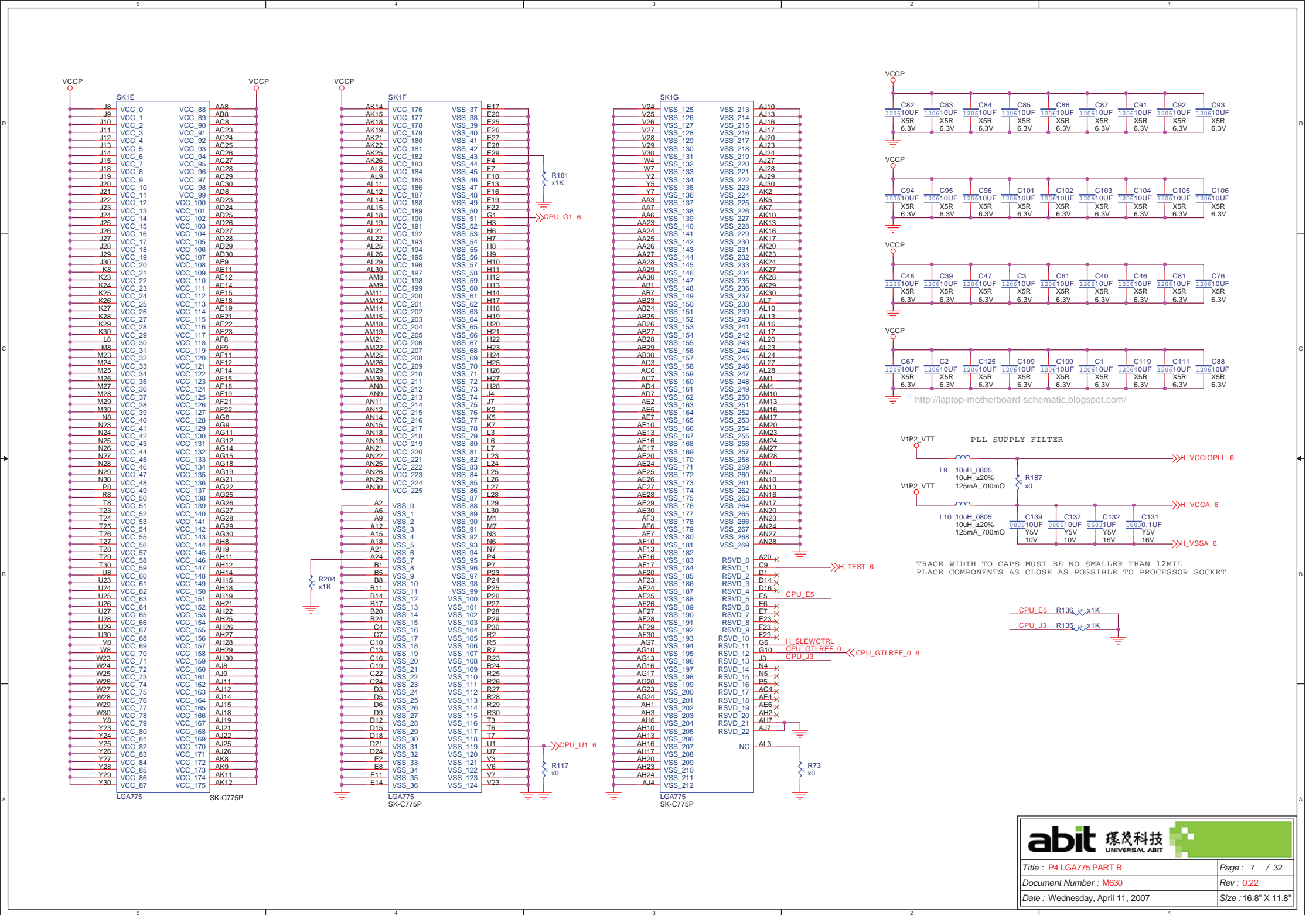
	SRC0	SRC1	SRC2	SRC3	SRC4	SRC5	SRC6	SRC7	SRC8	SRC9	SRC10	SRC11
PCIE X16										X		
PCIE X1 S1								X				
PCIE X1 S2	X											
PCIE MCH											X	
PCIE ICH					X							
ICH SATA			X									
JMB363			X									
G-LAN								X				

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CLK GROUP2 ROUTE

	PCI0	PCI1	PCI2	PCI3	PCI4	PCI5	USB48	REF14
PCI S1			X					
PCI S2				X				
PCI S3		X						
ICH						X		
FWH	X							
SIO	X							
1394				X				
SIO48							X	
ICH48							X	
ICH14								X





9,11 M_MAA_A[0..14] >> M_MAA_A[0..14]

9,12 M_MAA_B[0..14] >> M_MAA_B[0..14]

M_MAA_A0 R168 33 0402
M_MAA_A1 R186 33 0402
M_MAA_A2 R190 33 0402
M_MAA_A3 R194 33 0402
M_MAA_A4 R197 33 0402
M_MAA_A5 R201 33 0402
M_MAA_A6 R199 33 0402
M_MAA_A7 R207 33 0402
M_MAA_A8 R203 33 0402
M_MAA_A9 R209 33 0402
M_MAA_A10 R169 33 0402
M_MAA_A11 R211 33 0402
M_MAA_A12 R214 33 0402
M_MAA_A13 R150 33 0402
M_MAA_A14 R221 33 0402

9,11 M_SBA_A0 >> R166 33 0402
9,11 M_SBA_A1 >> R171 33 0402
9,11 M_SBA_A2 >> R218 33 0402
9,11 M_WE_A >> R161 33 0402
9,11 M_RAS_A >> R163 33 0402
9,11 M_CAS_A >> R149 33 0402

9,11 M_SODT_A0 >> R153 43 0402
9,11 M_SODT_A1 >> R146 43 0402
9,11 M_SODT_A2 >> R155 43 0402
9,11 M_SODT_A3 >> R144 43 0402

9,11 M_SCKE_A0 >> R227 43 0402
9,11 M_SCKE_A1 >> R230 43 0402
9,11 M_SCKE_A2 >> R224 43 0402
9,11 M_SCKE_A3 >> R233 43 0402

9,11 M_SCS_A0 >> R157 43 0402
9,11 M_SCS_A1 >> R151 43 0402
9,11 M_SCS_A2 >> R159 43 0402
9,11 M_SCS_A3 >> R148 43 0402

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M_MAA_B0 R184 33 0402
M_MAA_B1 R196 33 0402
M_MAA_B2 R193 33 0402
M_MAA_B3 R198 33 0402
M_MAA_B4 R200 33 0402
M_MAA_B5 R202 33 0402
M_MAA_B6 R206 33 0402
M_MAA_B7 R210 33 0402
M_MAA_B8 R208 33 0402
M_MAA_B9 R213 33 0402
M_MAA_B10 R177 33 0402
M_MAA_B11 R215 33 0402
M_MAA_B12 R217 33 0402
M_MAA_B13 R160 33 0402
M_MAA_B14 R220 33 0402

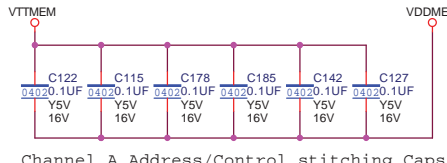
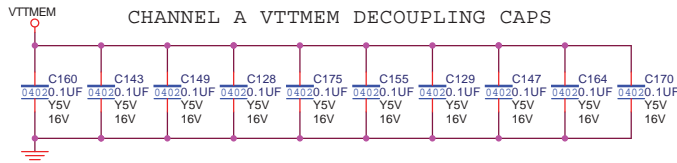
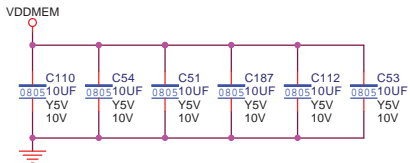
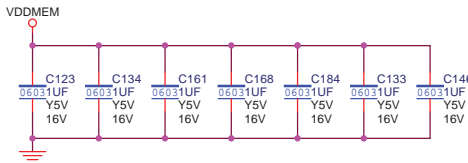
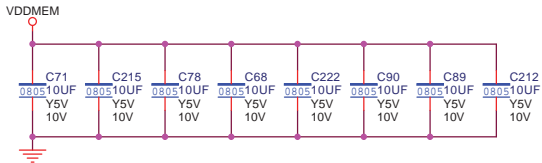
9,12 M_SBA_B0 >> R176 33 0402
9,12 M_SBA_B1 >> R179 33 0402
9,12 M_SBA_B2 >> R222 33 0402

9,12 M_WE_B >> R170 33 0402
9,12 M_RAS_B >> R173 33 0402
9,12 M_CAS_B >> R164 33 0402

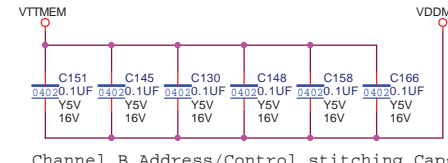
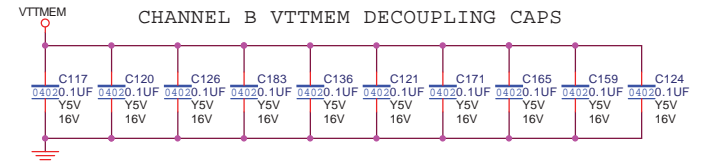
9,12 M_SODT_B0 >> R147 43 0402
9,12 M_SODT_B1 >> R145 43 0402
9,12 M_SODT_B2 >> R162 43 0402
9,12 M_SODT_B3 >> R154 43 0402

9,12 M_SCKE_B0 >> R226 43 0402
9,12 M_SCKE_B1 >> R235 43 0402
9,12 M_SCKE_B2 >> R232 43 0402
9,12 M_SCKE_B3 >> R228 43 0402

9,12 M_SCS_B0 >> R158 43 0402
9,12 M_SCS_B1 >> R156 43 0402
9,12 M_SCS_B2 >> R167 43 0402
9,12 M_SCS_B3 >> R152 43 0402

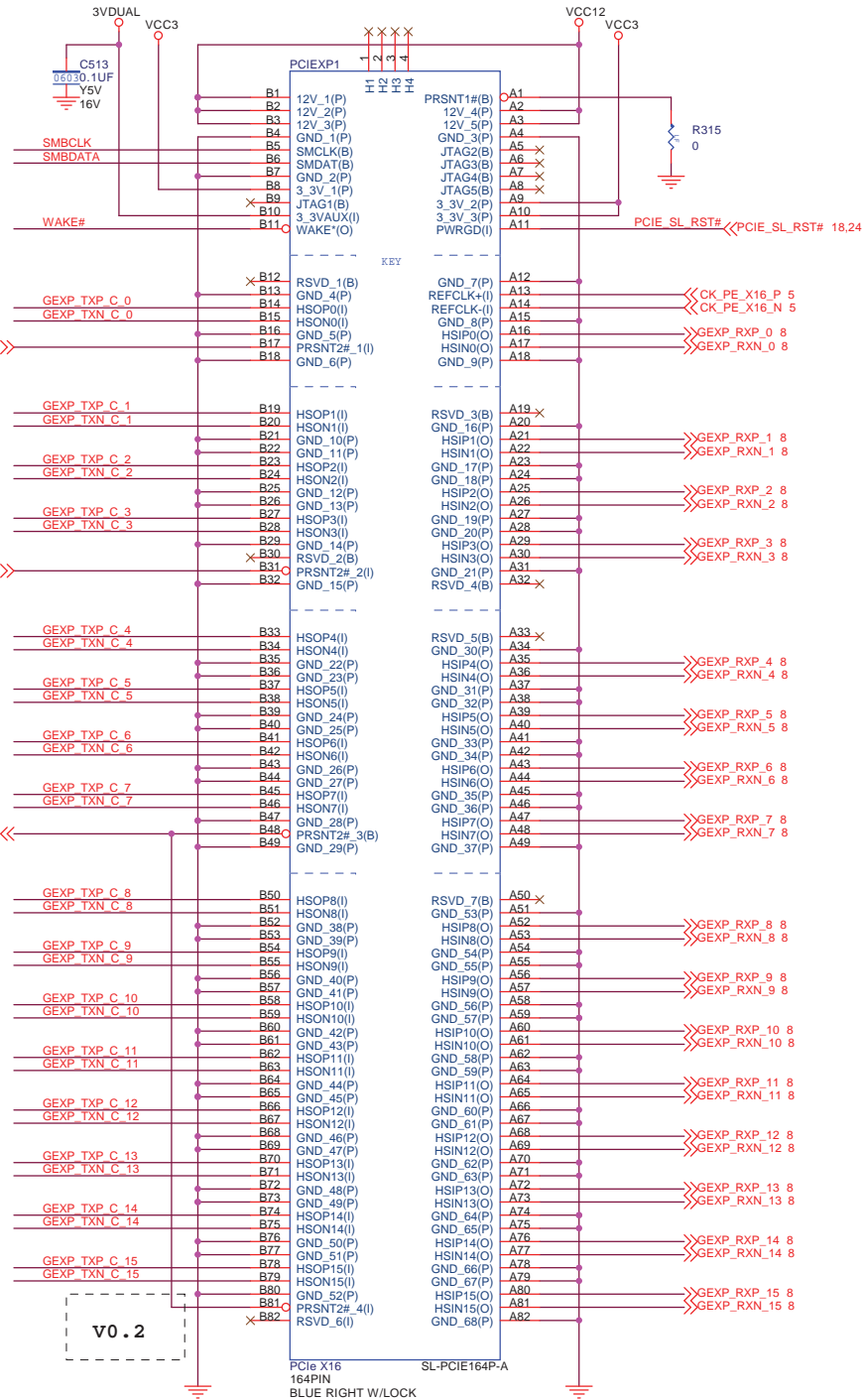


place at left
and right ends
of VTT island



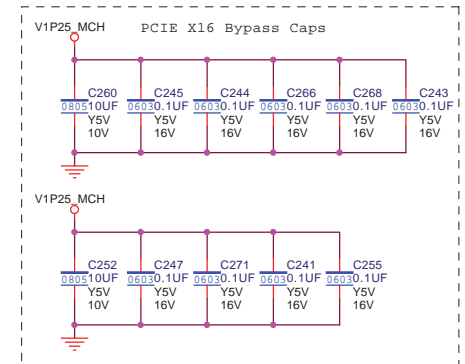
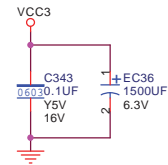
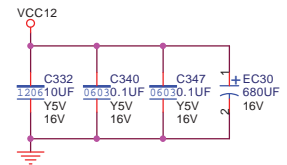
place at left
and right ends
of VTT island

8 GEXP_RXP_0.7 << GEXP_RXP_0.7
8 GEXP_RXN_0.7 << GEXP_RXN_0.7
8 GEXP_RXP_8.15 << GEXP_RXP_8.15
8 GEXP_RXN_8.15 << GEXP_RXN_8.15
8 GEXP_TXP_0 >> C293 0.1UF GEXP_TXP_C_0
8 GEXP_TXN_0 >> C292 0.1UF GEXP_TXN_C_0
8 GEXP_TXP_1 >> C294 0.1UF GEXP_TXP_C_1
8 GEXP_TXN_1 >> C295 0.1UF GEXP_TXN_C_1
8 GEXP_TXP_2 >> C296 0.1UF GEXP_TXP_C_2
8 GEXP_TXN_2 >> C297 0.1UF GEXP_TXN_C_2
8 GEXP_TXP_3 >> C298 0.1UF GEXP_TXP_C_3
8 GEXP_TXN_3 >> C299 0.1UF GEXP_TXN_C_3
8 GEXP_TXP_4 >> C300 0.1UF GEXP_TXP_C_4
8 GEXP_TXN_4 >> C301 0.1UF GEXP_TXN_C_4
8 GEXP_TXP_5 >> C303 0.1UF GEXP_TXP_C_5
8 GEXP_TXN_5 >> C302 0.1UF GEXP_TXN_C_5
8 GEXP_TXP_6 >> C305 0.1UF GEXP_TXP_C_6
8 GEXP_TXN_6 >> C304 0.1UF GEXP_TXN_C_6
8 GEXP_TXP_7 >> C307 0.1UF GEXP_TXP_C_7
8 GEXP_TXN_7 >> C306 0.1UF GEXP_TXN_C_7
8 GEXP_TXP_8 >> C308 0.1UF GEXP_TXP_C_8
8 GEXP_TXN_8 >> C309 0.1UF GEXP_TXN_C_8
8 GEXP_TXP_9 >> C310 0.1UF GEXP_TXP_C_9
8 GEXP_TXN_9 >> C311 0.1UF GEXP_TXN_C_9
8 GEXP_TXP_10 >> C313 0.1UF GEXP_TXP_C_10
8 GEXP_TXN_10 >> C312 0.1UF GEXP_TXN_C_10
8 GEXP_TXP_11 >> C315 0.1UF GEXP_TXP_C_11
8 GEXP_TXN_11 >> C314 0.1UF GEXP_TXN_C_11
8 GEXP_TXP_12 >> C317 0.1UF GEXP_TXP_C_12
8 GEXP_TXN_12 >> C316 0.1UF GEXP_TXN_C_12
8 GEXP_TXP_13 >> C319 0.1UF GEXP_TXP_C_13
8 GEXP_TXN_13 >> C318 0.1UF GEXP_TXN_C_13
8 GEXP_TXP_14 >> C321 0.1UF GEXP_TXP_C_14
8 GEXP_TXN_14 >> C320 0.1UF GEXP_TXN_C_14
8 GEXP_TXP_15 >> C323 0.1UF GEXP_TXP_C_15
8 GEXP_TXN_15 >> C322 0.1UF GEXP_TXN_C_15

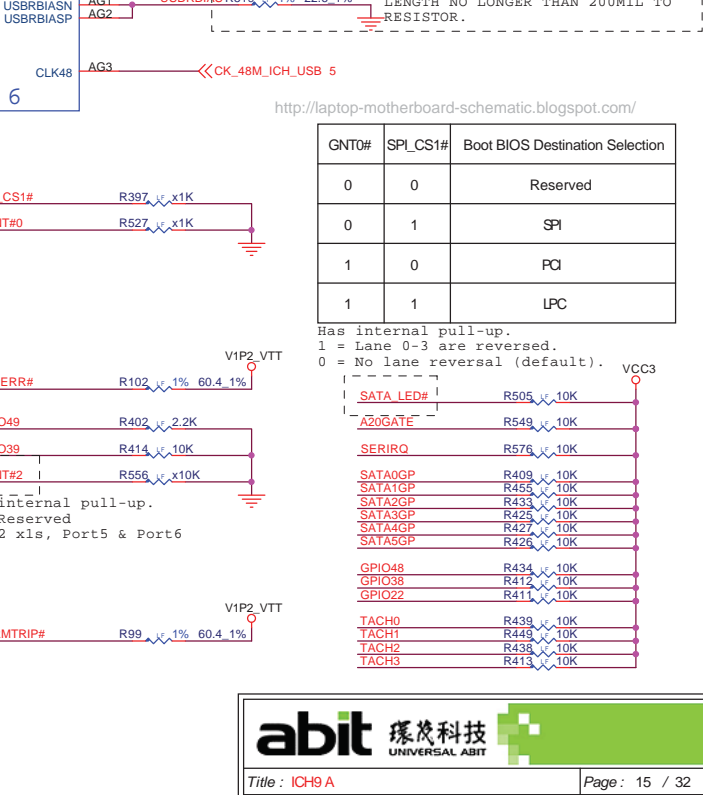
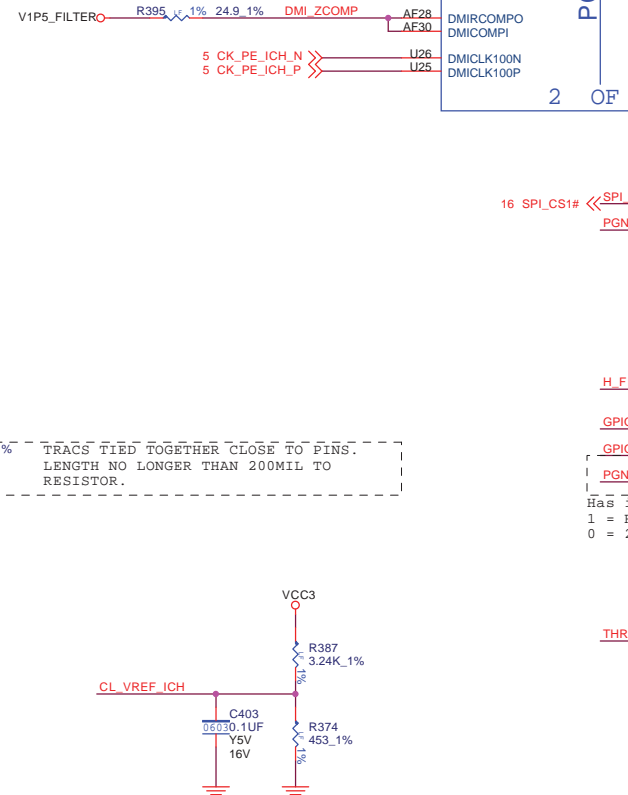
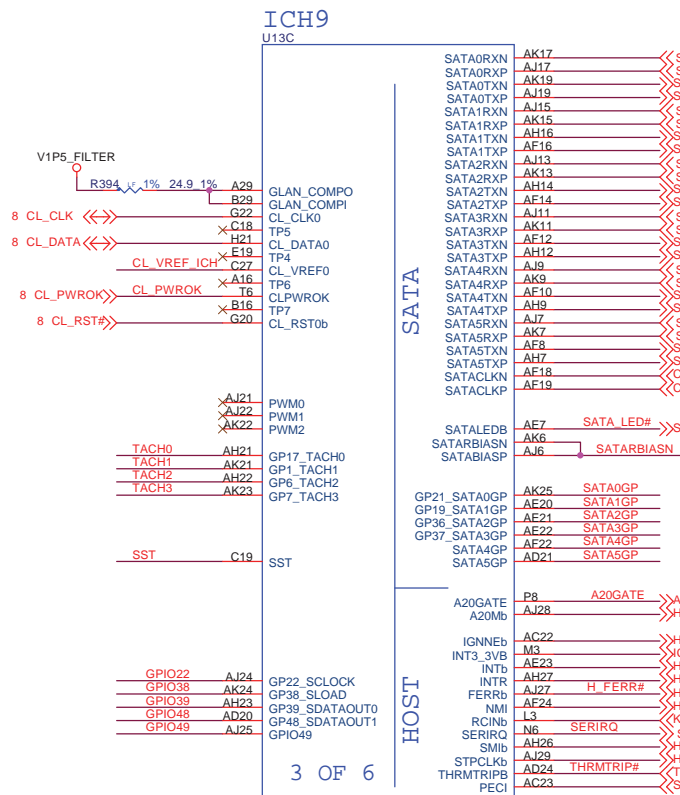
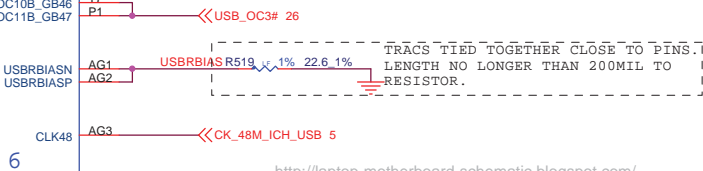
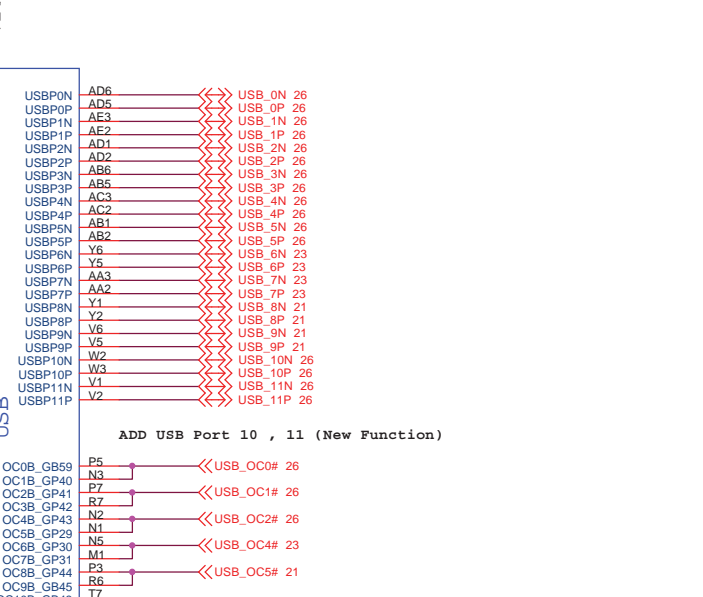
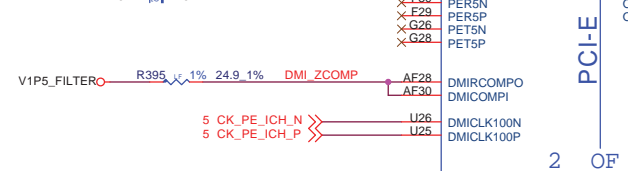
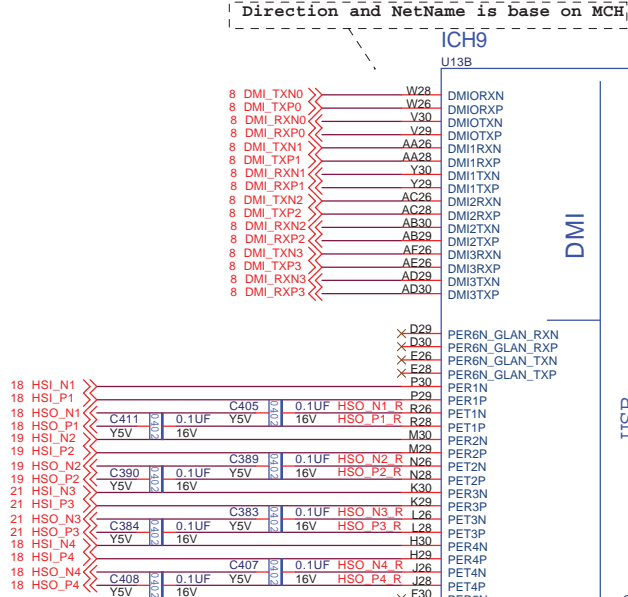
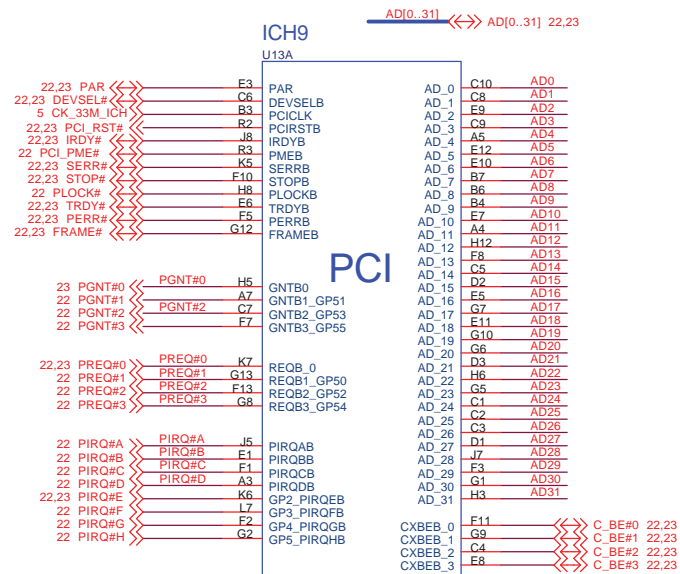


WAKE# >> WAKE# 16,18

SMBDATA << SMBDATA 5.11,12,16,18,22,25,28
SMBCLK << SMBCLK 5.11,12,16,18,22,25,28



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GNT0#	SPI_CS1#	Boot BIOS Destination Selection
0	0	Reserved
0	1	SPI
1	0	PCI
1	1	LPC

Has internal pull-up.
1 = Lane 0-3 are reversed.
0 = No lane reversal (default).

VCC3

SATA LED#

SERIRO

SATA0GP

SATA1GP

SATA2GP

SATA3GP

SATA4GP

SATA5GP

GPI048

GPI038

GPI022

TACH0

TACH1

TACH2

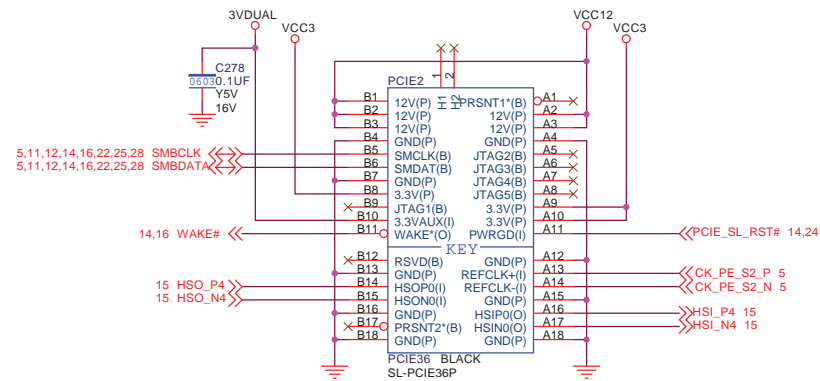
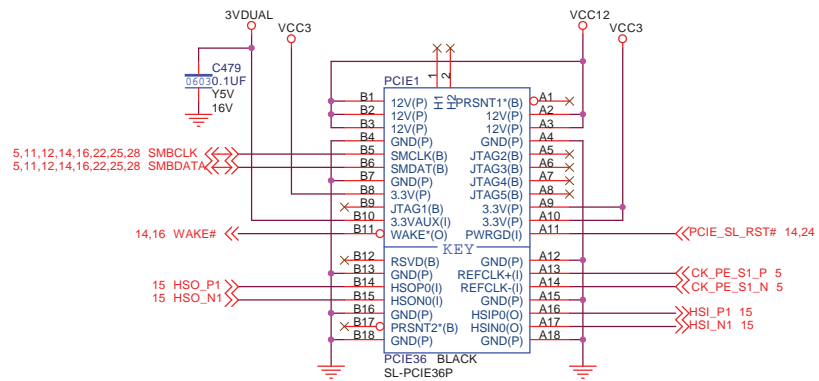
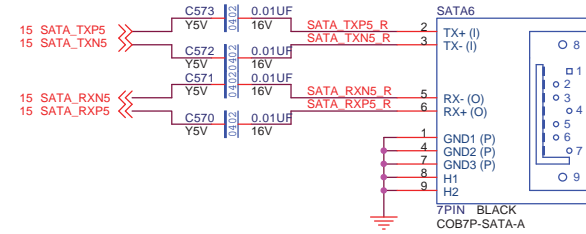
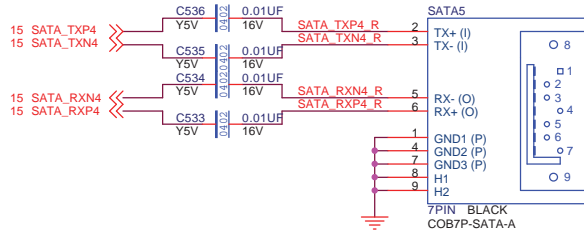
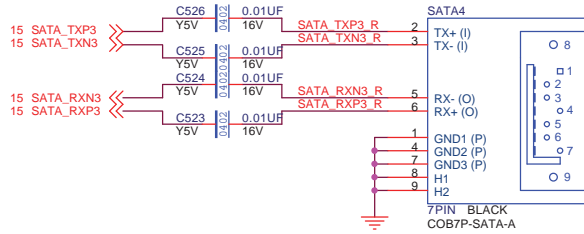
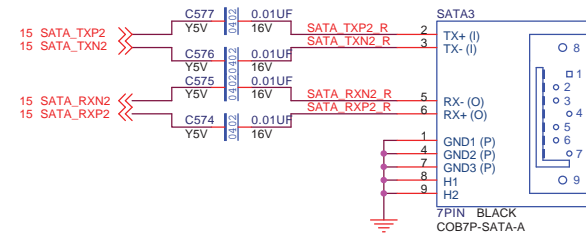
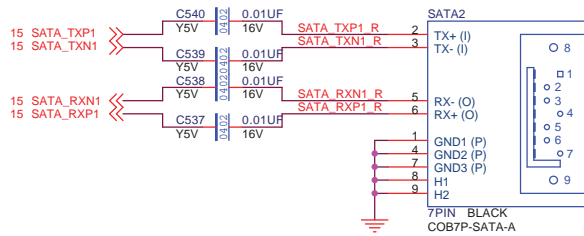
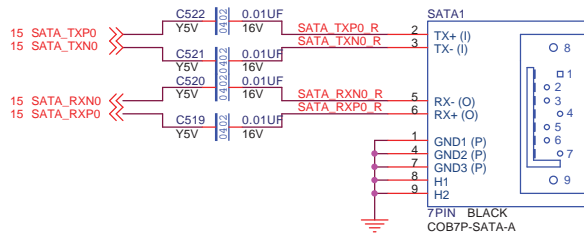
TACH3

abitt 環球科技 UNIVERSAL ABIT

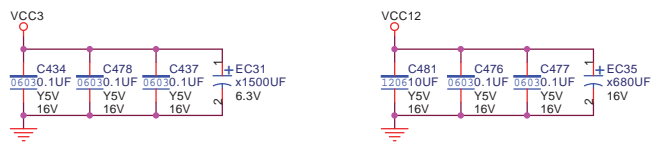
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Document Number : M630 Rev : 0.22

Date : Wednesday, April 11, 2007 Size : 16.8" X 11.8"



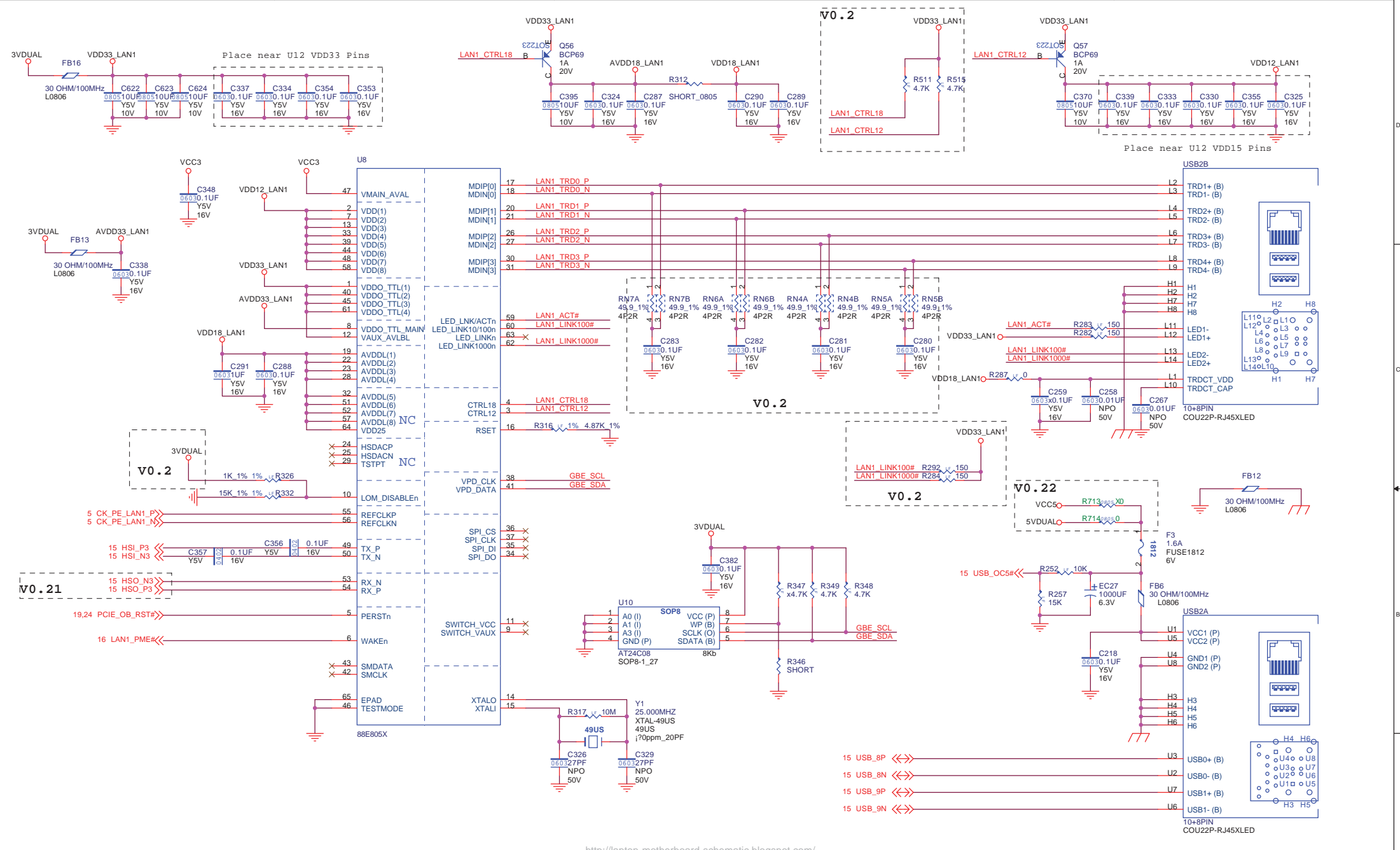
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FOR PCI EXPRESS X1 SLOT 1

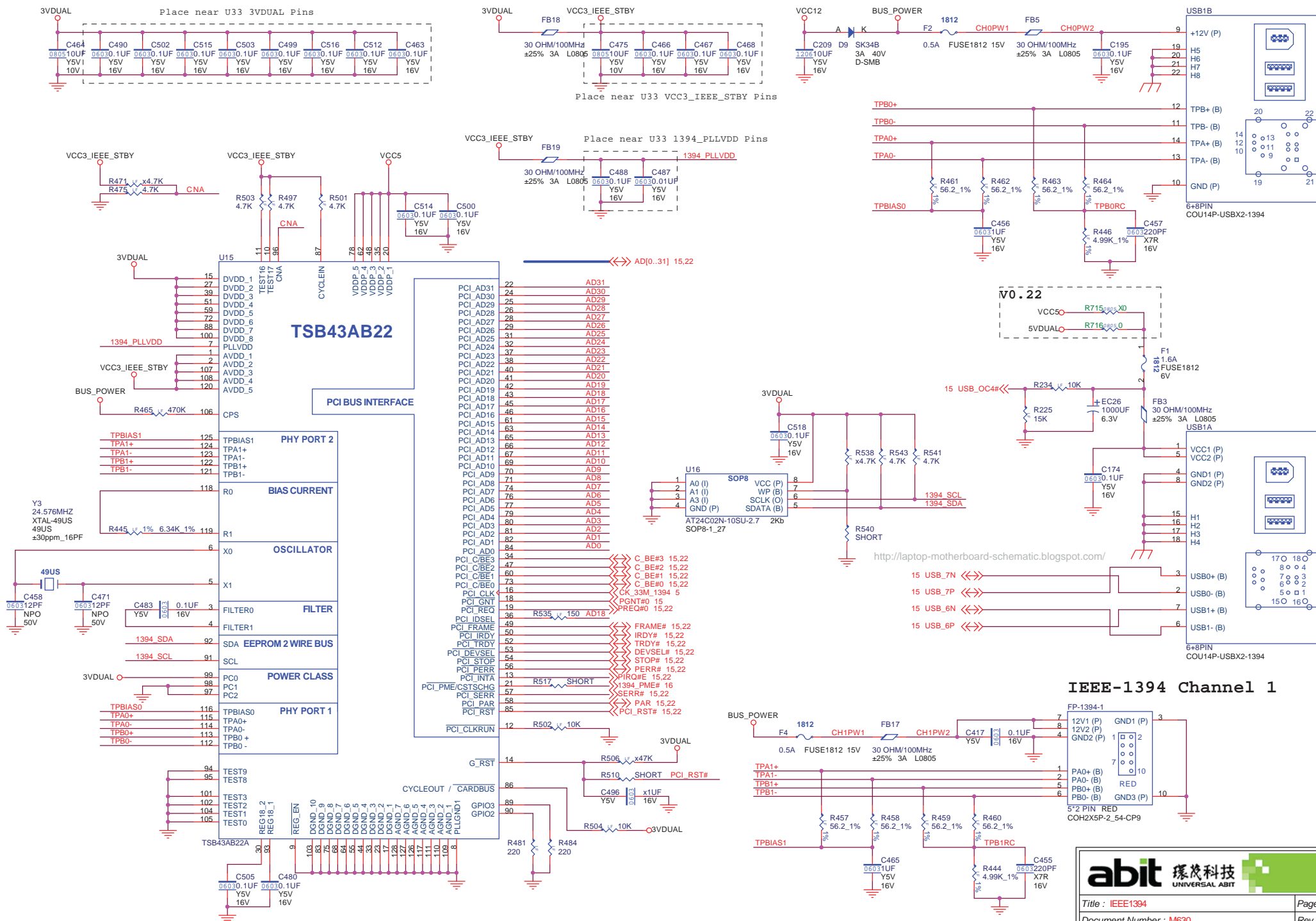


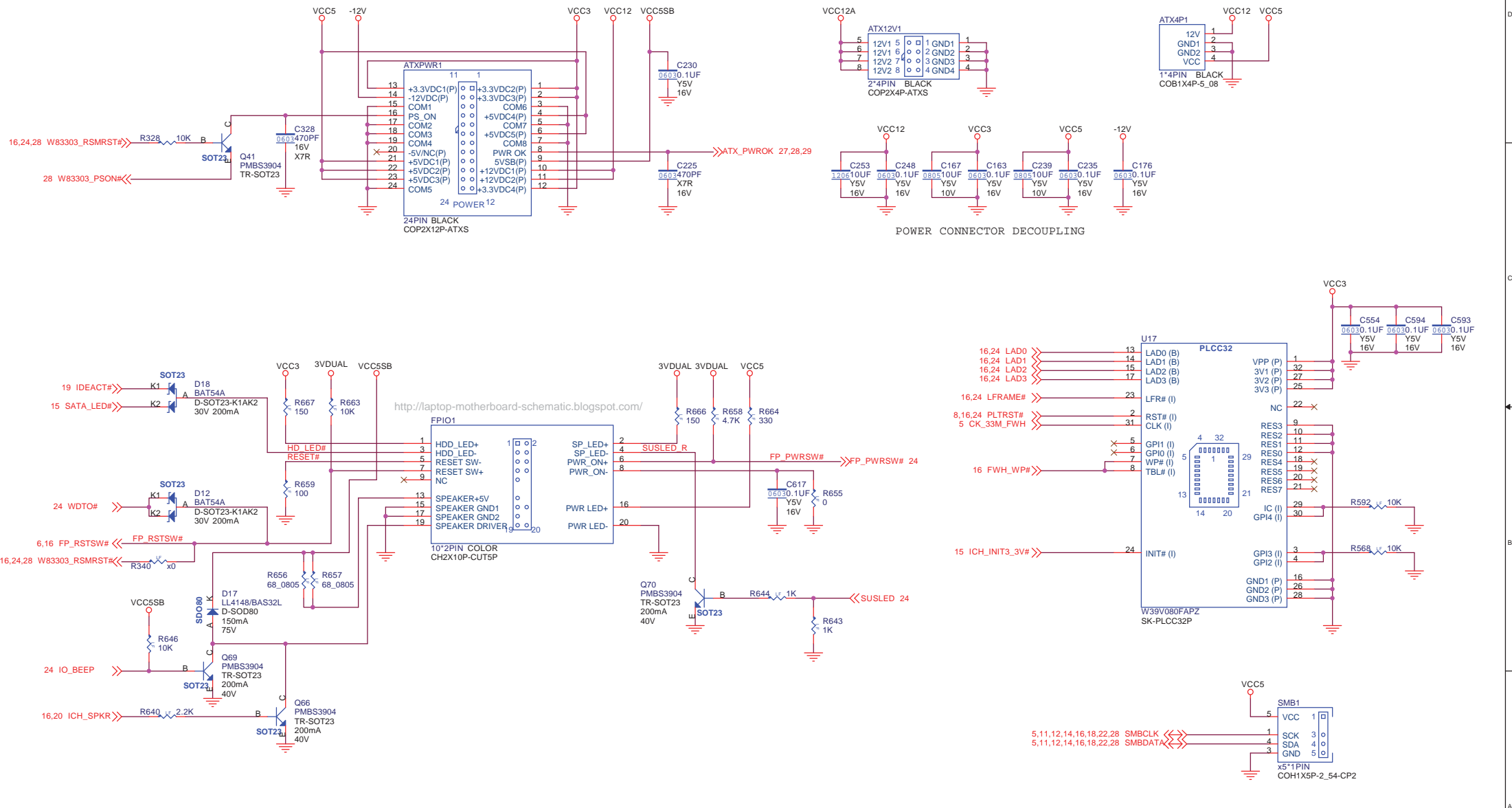
FOR PCI EXPRESS X1 SLOT 2

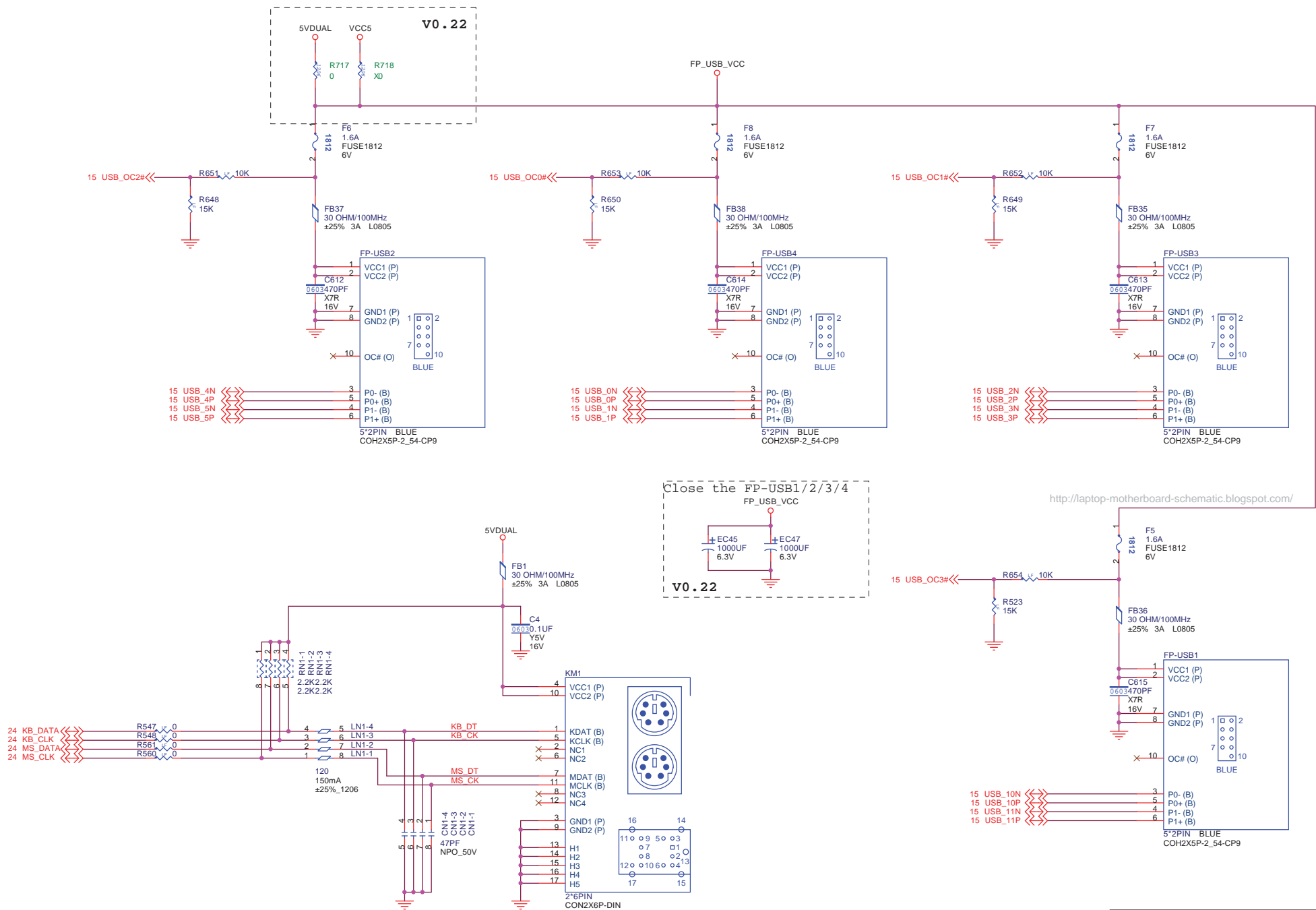


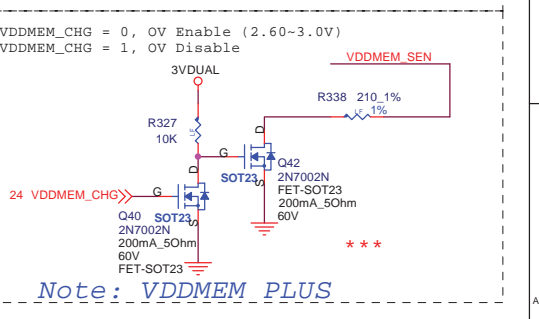
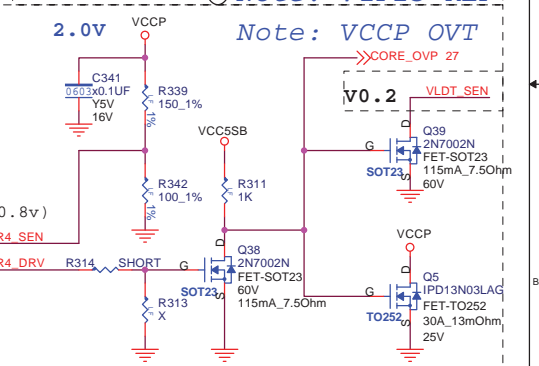
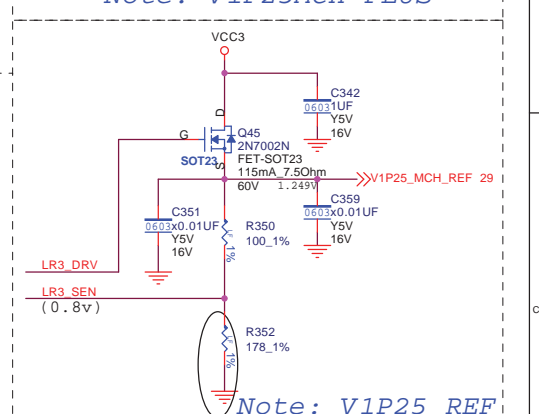
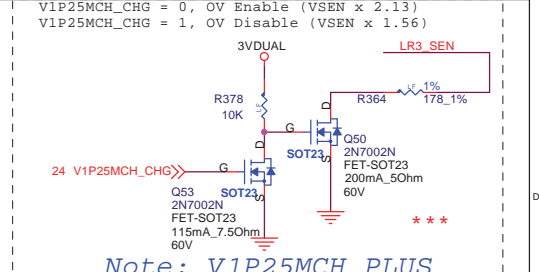
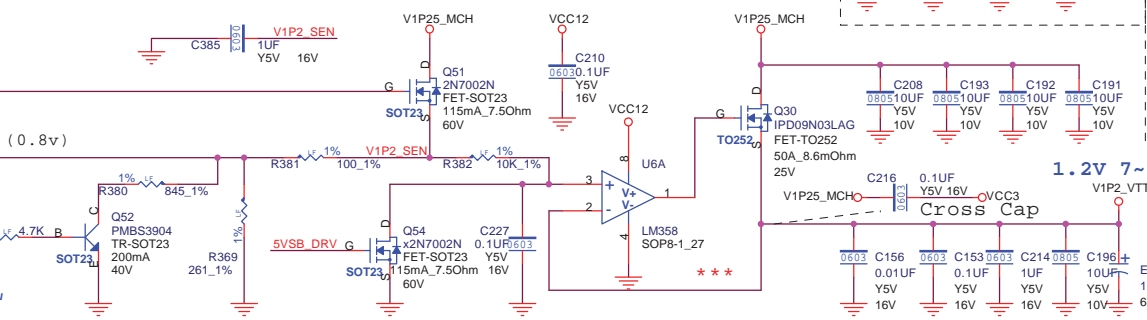
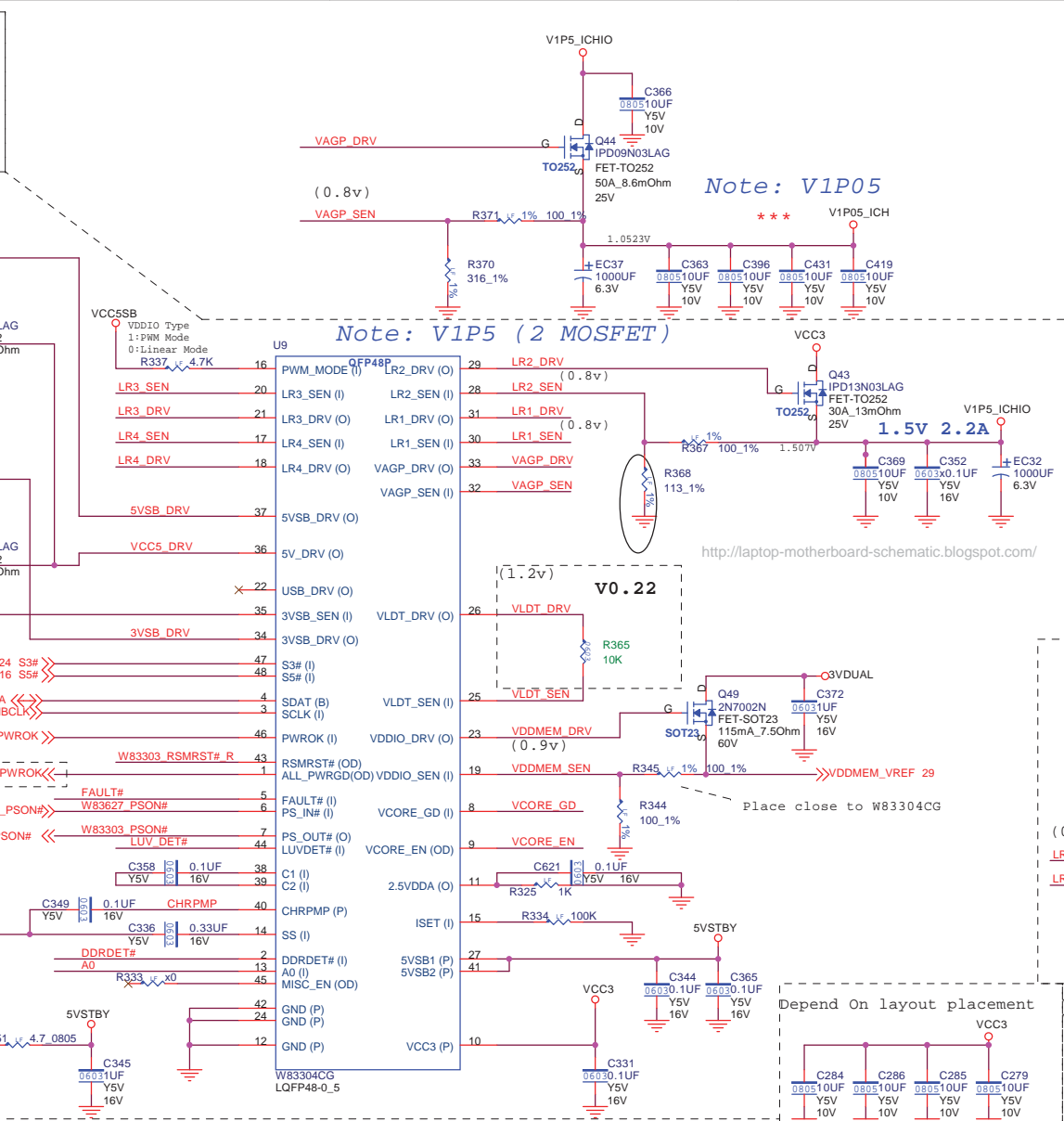
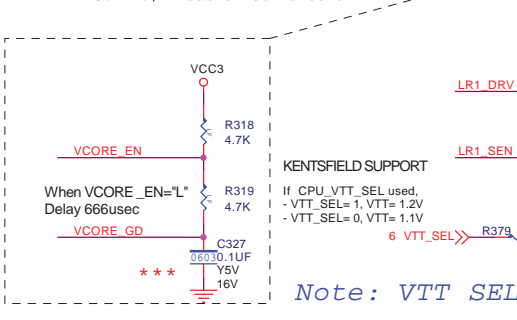
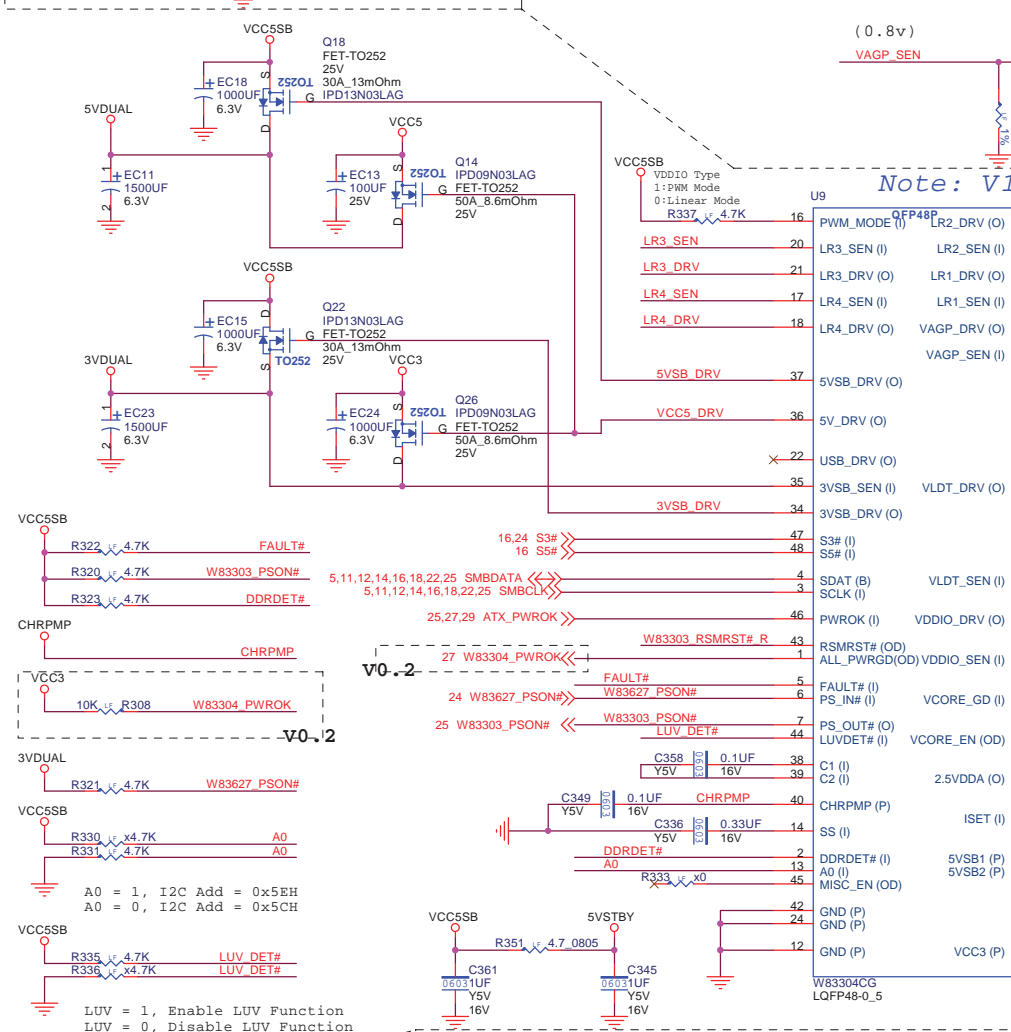
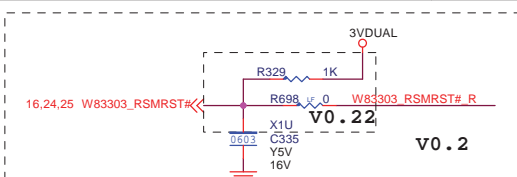
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IEEE-1394 Channel 0

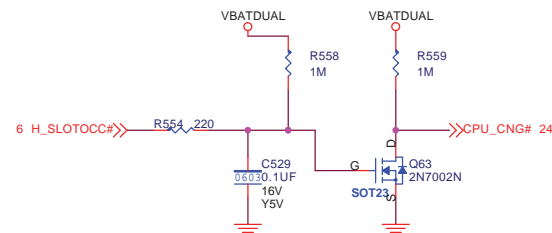
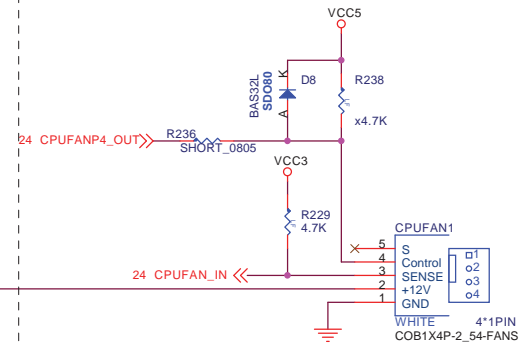
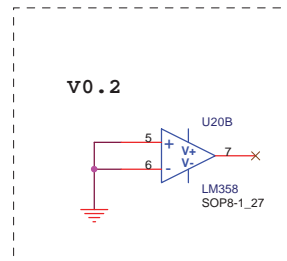
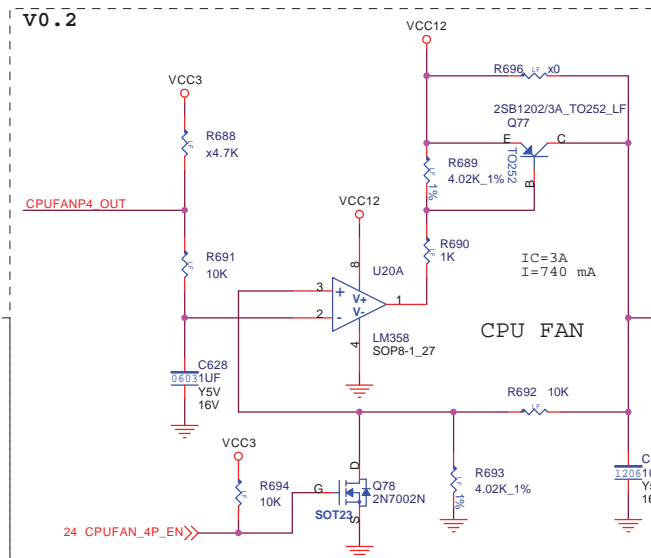
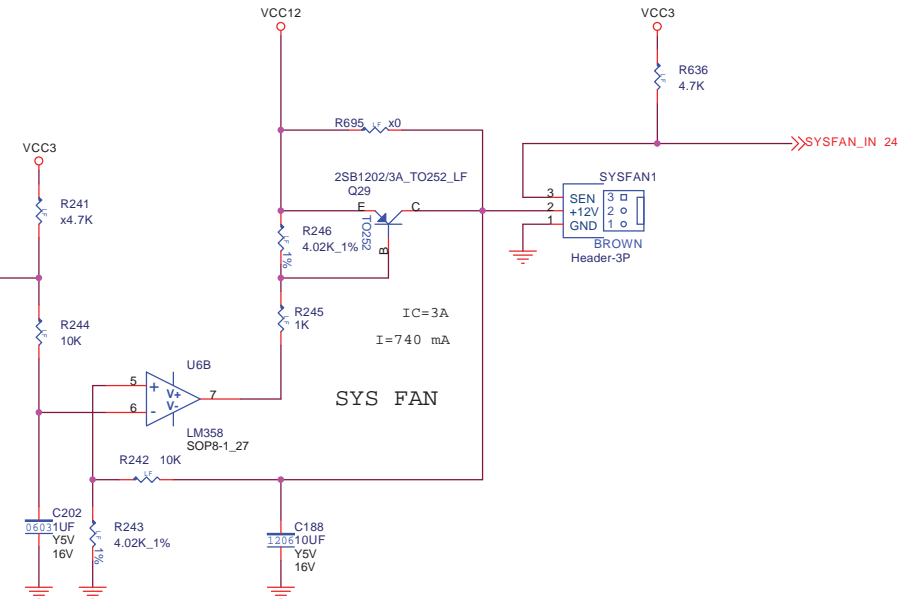
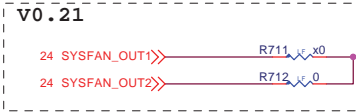
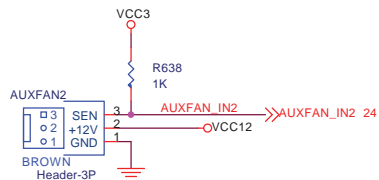
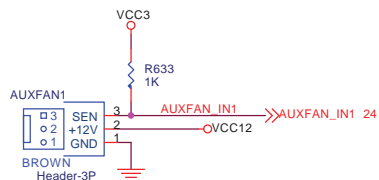
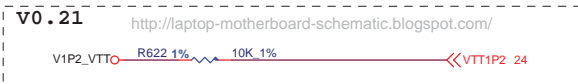
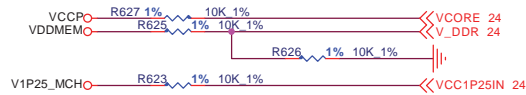
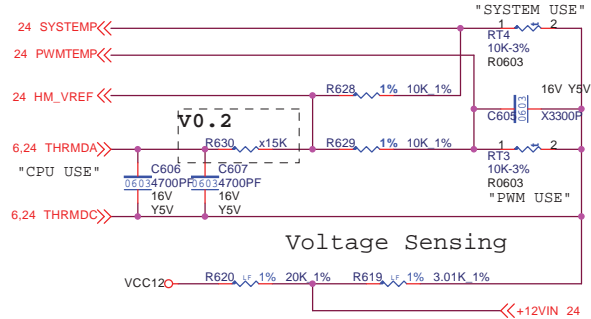


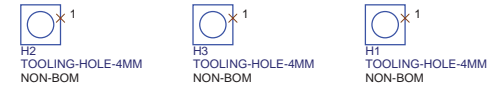
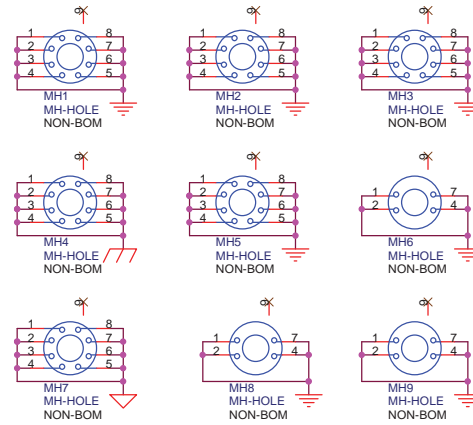
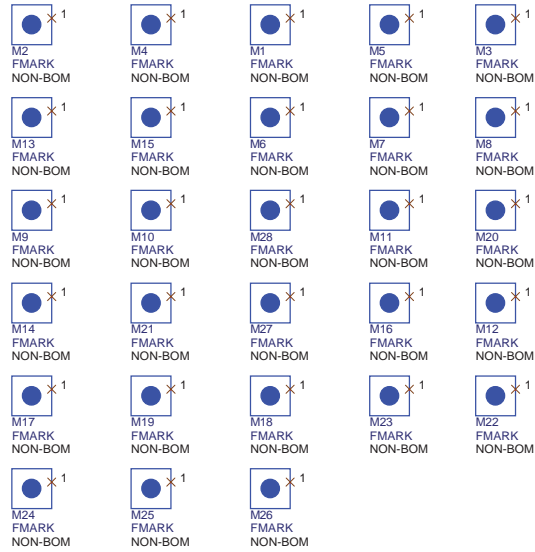
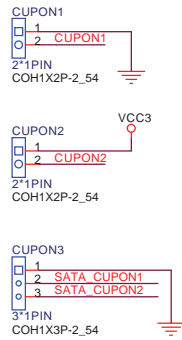




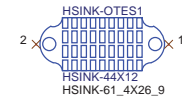
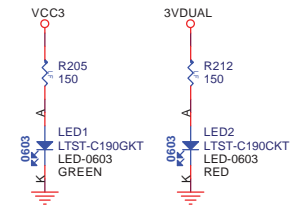
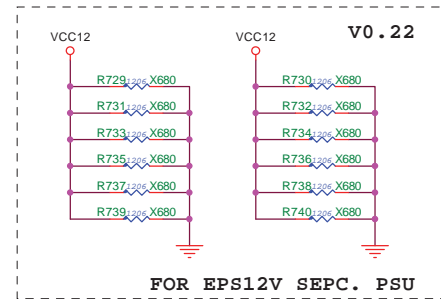


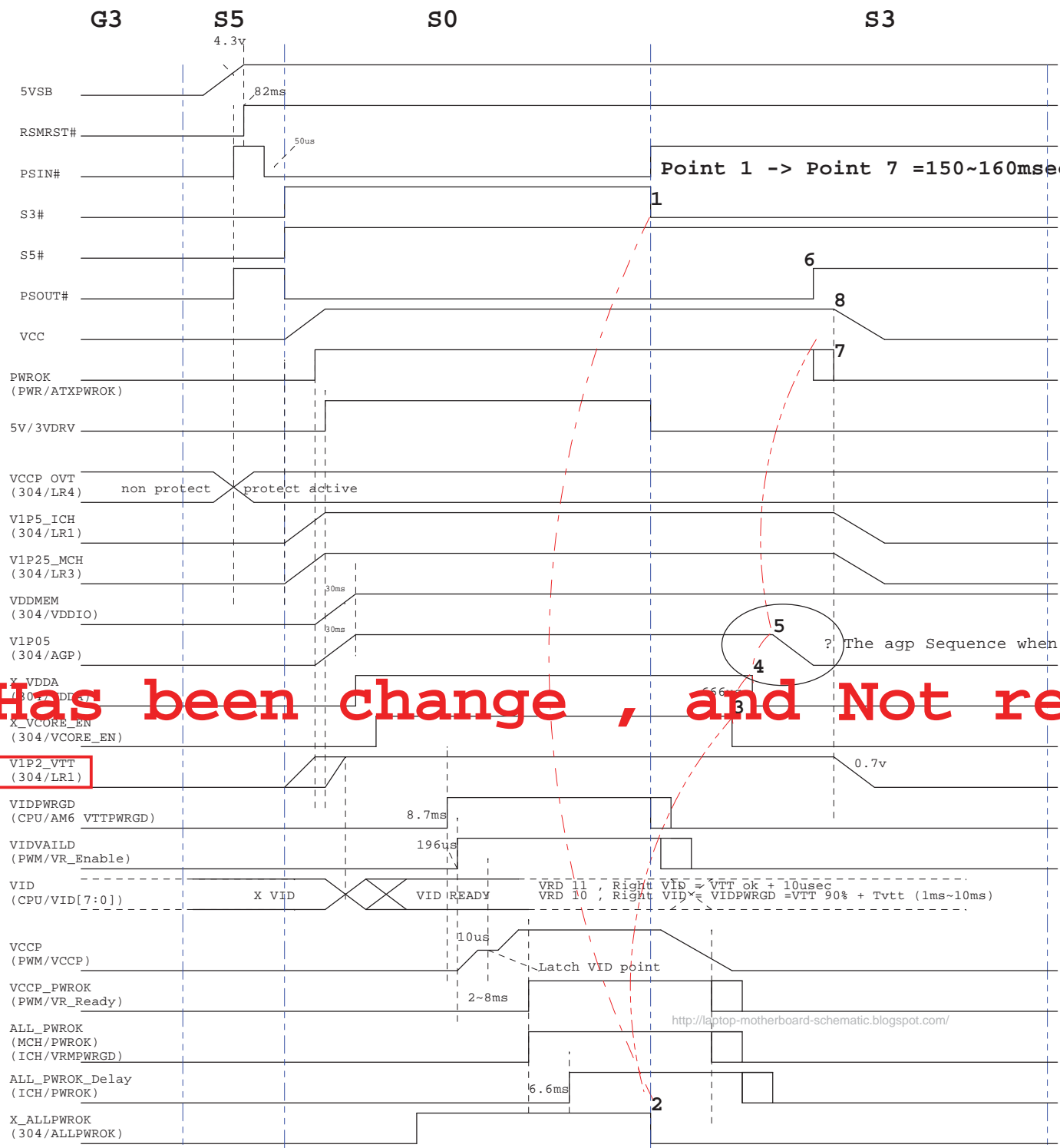
Temperature Sensing





<http://laptop-motherboard-schematic.blogspot.com/>





- V0.1 to V0.2 Bug List**
- *1.NB/SB CLPWRDG driving from "ALL PWROK_Delay".
 - *2.VID_VAILD SEQ Conrtoller = VTT and 304_ALLPWRFG.
 - 3.Layout issue, 5VDUAL not good arround PS2 KB/MS.
 - 4.LAN , RN4,5,6,7,C280,281,282,283 stuff.
 - 5.R_CPU_FSA,B schematic error, cross issue.
 - 6.BOOTSEL do not stuff any resistor.
 - 7.JMB368 Reset circuit fix.
 - 8.RTC RST# Dll remove.
 - 9.R516 changed from 1k to 10 ohm.
 - 10.CPU Thermal THRMADA# do no stupp pull high for Current mode detect.
 - 11.DC to DC Protect Fault circuit chagne design.
 - 12.VCCP ADJ 2.3.4 line cross problem fix.
 - 13.LAN VDD18,12 LDO Q56,Q57 B-E 4.7K stuff.
 - 14.R617 Change Pull high source from 3VDUAL to VCC3.
 - 15.GTLREF 2 and 3 name exchange.(correct it).
 - 16.Add GTLREF adjustable function..
 - 17.Modify the CPU FAN circuit for 4/3 Pin compatible.
 - 18.Add SPI Schematic.
 - 19.Solve the Wake on Lan issue, R326 Pull high to 3VDUAL.
 - 20.LAN_Link LED driver need ext-Pull UP to 3V.

- V0.1 to V0.2 Bug List**
- 1.GLAN HSO_P3 and HSO_N3 Signal route exchange.
 - 2.ICH VRM_PWROK connect to VCCP_PWROK for solve USB detect problem.

Has been change , and Not ready now !!!

VLDT By PASS